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Asymmetrical Cascade Multilevel Inverter for Higher Output Voltage Levels

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Abstract: Now a days the growth of interest in multilevel inverters has been increasing because there are enormous applications of there in FACTS and industrial drives etc., Although there are many topologies of multilevel inverters in literature, popular among them are cascaded H-bridge. In general the control methods of these cascaded inverters are designed an assumption of having all dc source voltages same for all H-bridges. This paper discusses the abilities of cascaded multilevel inverter to produce more output voltage levels with same number of H-bridges, but with different input voltage ratios. The ideal nature of input dc voltage sources is shown as an advantage in this paper. To propose a single- phase 27-level and 33-level asymmetrical cascaded H-bridge inverter. The output voltage of three phase Asymmetrical 27-level CHB gives 12.56% THD, whereas 33-level asymmetrical CHB gives 9.16% THD

Keywords: —Asymmetrical cascaded multilevel inverter,induction motor, and pulse width modulation technique.

1. INTRODUCTION:

Asymmetric voltage technology is used in the cascade H-bridge multilevel inverter to allow more levels of output voltage, so the cascade H bridge multilevel inverter is suitable for applications with increased voltage levels. Two H bridge inverters with a dc bus voltage of multiple relationships can be connected in cascade.Multilevel inverters have received added awareness for their ability on high-power and medium voltage function and because of former compensation such as high power quality, lower order harmonics, minimum switching losses and improved electromagnetic interference. And also multilevel inverters are promising; they have virtually sinusoidal output-voltage waveforms, Output current with improved harmonic profile, a lesser amount of stressing of electronic components owing to decreased voltages, switching losses that are inferior than those of predictable two-level inverters, a slighter filter size, and worse EMI, all of which make them cheaper, lighter, and more compact Multilevel inverters make small Common mode voltage; consequently the stress in the bearings of a motor allied to a multilevel motor drive can be condensed. In addition CM voltages can be eliminated by using advanced modulation technique. Multilevel inverters can draw input current with low distortion. These inverters can operate at equally fundamental frequency and high switching frequency PWM this project discusses the abilities of cascaded multilevel inverter to produce more output voltage levels with same number of H-bridges, but with different input voltage ratios. The ideal nature of input dc voltage sources is shown as an advantage. The proposed inverter is then used to feed an induction motor drive and the simulation results are obtained

CIRCUIT DIAGRAM:

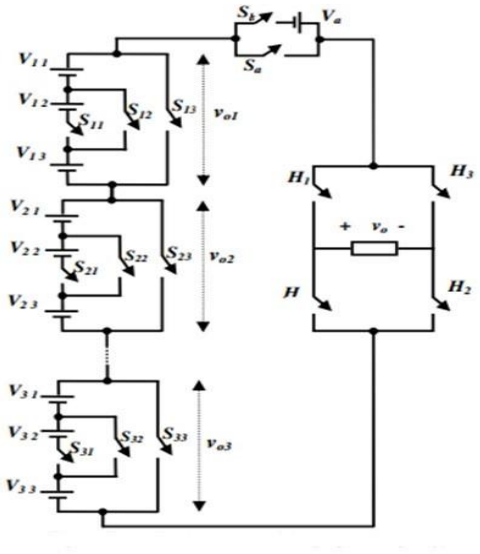


Fig.1. Generalized structure of the proposed topology

ii. MULTILEVEL INVERTER STRUCTURES:

Multilevel Inverter structures a voltage level of three is considered to be the smallest number in multilevel converter topologies. Due to the bi-directional switches, the multilevel VSC can work in both rectifier and inverter modes. This is why most of the time it is referred to as a converter instead of an inverter in this dissertation. A multilevel converter can switch either its input or output nodes (or both) between multiple (more than two) levels of voltage or current. As the number of levels reaches infinity, the output THD approaches zero. The number of the achievable voltage levels, however,

is limited by voltage-imbalance problems, voltage clamping requirements, circuit layout and packaging constraints complexity of the controller, and, of course, capital and maintenance costs.

iii. CASCADED H-BRIDGEMULTILEVEL INVERTER:

One of the basic and well-known topologies among all multilevel inverters is Cascaded Multilevel Inverter. It can be used for both single and three phase conversion. It uses H-Bridge including switches and diodes. At least three voltage levels are required for a multilevel inverter. This can be accomplished by a single H-Bridge unit in Cascaded H-Bridge Multilevel Inverter. To keep the discussion snappy and clear I will go with the major points of this topology and also its advantages and disadvantages compared to other topologies.

FEATURES OF CASCADED H-BRIDGEMULTILEVEL INVERTER:

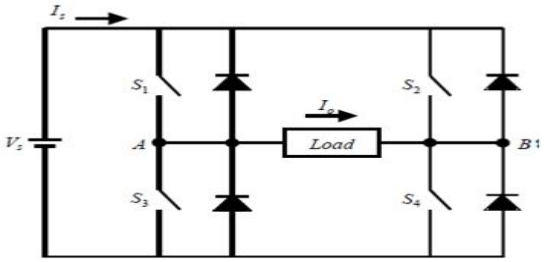


Fig.2. Basic CHB circuit

H-BRIDGE CELL:

Each H-Bridge Cell consists of four switches and four diodes as shown in the picture. Like every H-Bridge, different combinations of switch positions determine different voltages such as V+, V- and 0. Two switching combinations are present for 0 volts. S1 and S2 are connected to positive voltage and S3 and S4 are connected to negative voltage.

WHY CASCADED H-BRIDGE MULTILEVEL INVERTER?

Cascaded H-Bridge (CHB) configuration has recently become very popular in high power AC supplies and adjustable-speed drive applications. A cascade multilevel inverter consists of a series of H-bridge (single-phase full bridge) inverter units in each of its three Introduction 8 phases. Each H-bridge unit has its own dc source, which for an induction motor would be a battery unit, fuel cell or solar cell. Each SDC (separate D.C. source) is associated with a single phase full-bridge inverter. The ac terminal voltages of different level inverters are connected in series. Through different combinations of the four switches, S1-S4, each converter level can generate three different voltage outputs, +Vdc, -Vdc and zero. The AC outputs of different fullbridge converters in the same phase are connected in series such that the synthesized voltage waveform is the sum of the individual converter outputs. Note that the number of output-phase voltage levels is defined in a different way from those of the two previous converters (i.e. diode clamped and flying capacitor). In this topology, the number of output-phase voltage levels is defined by m= 2N+1, where N is the number of DC sources. A seven-level cascaded converter, for example, consists of three DC sources and three full bridge converters. Minimum harmonic distortion can be obtained by controlling the conducting angles at different converter levels. Each H- bridge unit generates a quasi-square waveform by phase shifting its positive and negative phase legs" switching timings.

ADVANTAGES:

- Lower THD
- Lower complexity
- Better voltage quality

PROPOSED CONCEPT:

The basic unit of the proposed topology is depicted. The basic unit has three unidirectional switches (S1, S2 andS3) and three dc sources (V1, V2 and V3). Switch S1 isconnected in series with the source V2 and switch S2 is connected across the source-switch assembly. Care must betaken that both the series and the parallel switch are not turnedon simultaneously. The remaining sources V1 and V 3 are connected in series on either side of the source-switchassembly.The basic unit can generate two distinct voltage levelsbesides zero. It can also be noted that only one of these threeswitches is turned on at any point in time to avoid shortcircuiting of the dc sources. As the lowest voltage that is generated by the basic unit is V1+V3 (2Vdc if V1 =V3 =Vdc), anauxiliary unit is required to generate lowest step (Vdc). The basic unit together with the auxiliary unit can generate allpositive the voltage steps.To generate the negative voltage steps, a polarity generatorcircuit (H-bridge) is connected with this basic-auxiliary unit assembly. The auxiliary unit and the H-bridge module the auxiliary unit has a dc voltage sourcewhose magnitude is equal to the lowest voltage step (Vdc) to

begenerated. In addition, two unidirectional switches (Sa and Sb)are provided to include or exclude the dc source from the restof the circuit The switching status and the voltage levels that can be generated.

iii.CONTROLSCHEME:

This section will discuss in detail a converter consisting of three modules withthese results in a huge number of diverse output voltage levels with an incredibly good voltage resolution. This composition will be compared with the predictable approach with identical DC voltage sources, and with the Hybrid Multilevel Inverter using a 1:3:9 voltage relation. Two different control methods for a single phase converter are offered. Both algorithms imagine a steady sampling interval of the control, Ts. The first one uses a stable switching state during a full sampling interval (step or staircase method), where as the second one is implemented with a Pulse Width Modulation (PWM method). Both methods receive that the DC source voltages are not steady but variable in time. The definite voltages on the capacitors are therefore calculated, and the phase voltage vector Vii is created. In order to compute all attainable output voltages Vol, the phase voltage vector is multiplied with all 31 possible switching states SI. This results in an unsorted vector containing all feasible output voltages

SWITCHING SEQUENCE OF 27-LEVEL CHB INVERTER:

TABLE II. SWITCHING SEQUNCE OF 27-LEVEL CHB INVERTER

Switches / Voltage Levels	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
V_{dc}	1	1	0	0	0	1	0	1	0	1	0	1
$2V_{dc}$	0	0	1	1	1	1	0	0	0	1	0	1
$3V_{dc}$	0	1	0	1	1	1	0	0	0	1	0	1
$4V_{dc}$	1	1	0	0	1	1	0	0	0	1	0	1
$5V_{dc}$	0	0	1	1	0	0	1	1	1	1	0	0
$6V_{dc}$	0	1	0	1	0	0	1	1	1	1	0	0
$7V_{dc}$	1	1	0	0	0	0	1	1	1	1	0	0
$8V_{dc}$	0	0	1	1	0	1	0	1	1	1	0	0
$9V_{dc}$	0	1	0	1	0	1	0	1	1	1	0	0
$10V_{dc}$	1	1	0	0	0	1	0	1	1	1	0	0
$11V_{dc}$	0	0	1	1	1	1	0	0	1	1	0	0
$12V_{dc}$	0	1	0	1	1	1	0	0	1	1	0	0
$13V_{dc}$	1	1	0	0	1	1	0	0	1	1	0	0
$0V_{dc}$	0	1	0	1	0	1	0	1	0	1	0	1
$-V_{dc}$	0	0	1	1	0	1	0	1	0	1	0	1
$-2V_{dc}$	1	1	0	0	0	0	1	1	0	1	0	1
$-3V_{dc}$	0	1	0	1	0	0	1	1	0	1	0	1
$-4V_{dc}$	0	0	1	1	0	0	1	1	0	1	0	1
$-5V_{dc}$	1	1	0	0	1	1	0	0	0	0	1	1
$-6V_{dc}$	0	1	0	1	1	1	0	0	0	0	1	1
$-7V_{dc}$	0	0	1	1	1	1	0	0	0	0	1	1
$-8V_{dc}$	1	1	0	0	0	1	0	1	0	0	1	1
$-9V_{dc}$	0	1	0	1	0	1	0	1	0	0	1	1
$-10V_{dc}$	0	0	1	1	0	1	0	1	0	0	1	1
$-11V_{dc}$	1	1	0	0	0	0	1	1	0	0	1	1
$-12V_{dc}$	0	1	0	1	0	0	1	1	0	0	1	1
$-13V_{dc}$	0	0	1	1	0	0	1	1	0	0	1	1

SWITCHING SEQUENCE OF 33-LEVEL CHB INVERTER:

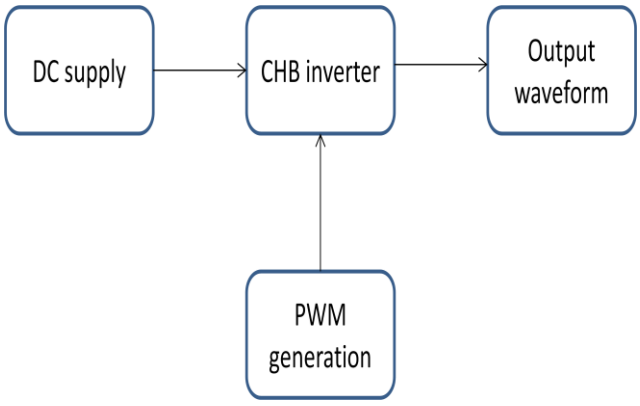
Status of switches and output voltage

Mode	Status of Switches									V_o
	S_1	S_2	S_3	S_a	S_b	H_1	H_2	H_3	H_4	
1	0	0	1	1	0	1	0	1	0	0
2	0	0	0	0	1	1	1	0	0	V_a
3	0	1	0	1	0	1	1	0	0	V_1+V_3
4	0	1	0	0	1	1	1	0	0	$V_a+V_1+V_3$
5	1	0	0	1	0	1	1	0	0	$V_1+V_2+V_3$
6	1	0	0	0	1	1	1	0	0	$V_a+V_1+V_2+V_3$
7	0	0	0	0	1	0	0	1	1	$-V_a$
8	0	1	0	1	0	0	0	1	1	$-(V_1+V_3)$
9	0	1	0	0	1	0	0	1	1	$-(V_a+V_1+V_3)$
10	1	0	0	1	0	0	0	1	1	$-(V_1+V_2+V_3)$
11	1	0	0	0	1	0	0	1	1	$-(V_a+V_1+V_2+V_3)$

v. SIMULATION RESULT:

The below figure shows the output wave forms theproposed asymmetrical converter. It is clearly seenthat the level of inverter varies with the change inthe ratios of input voltage. The inverter gives 27 level output voltage when the ratio is 4:5:6and it gives 27 level output voltage. This inverter having 3 bridges connectedin series gives different levels of output voltageswithout changing the circuit except the ratios of input voltages. Proposed system used 33 levels Switching of the converter is done by following the staircase control technique. Pulse width Modulation technique can also be applied byappropriate calculation of the switching timeperiod.

SIMULATION BLOCK DIAGRAM:



(a): 27 LEVEL SIMULATIONS AND OUTPUT:

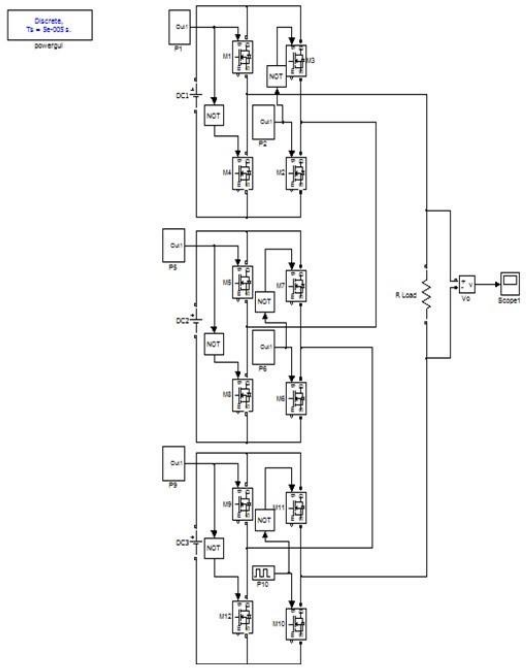


Fig.3. Proposed asymmetrical cascade multilevel inverter 27 level

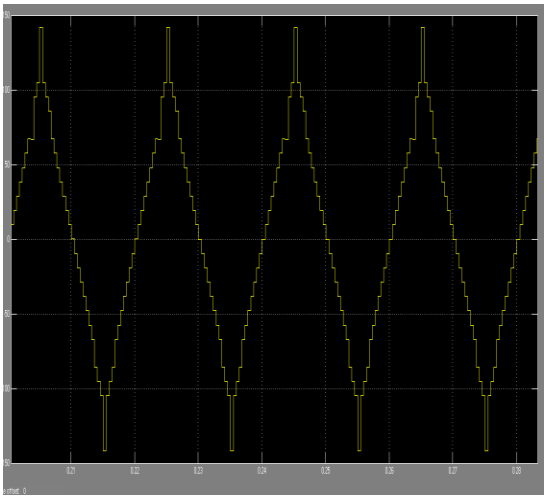


Fig.4. Simulation result 27 level

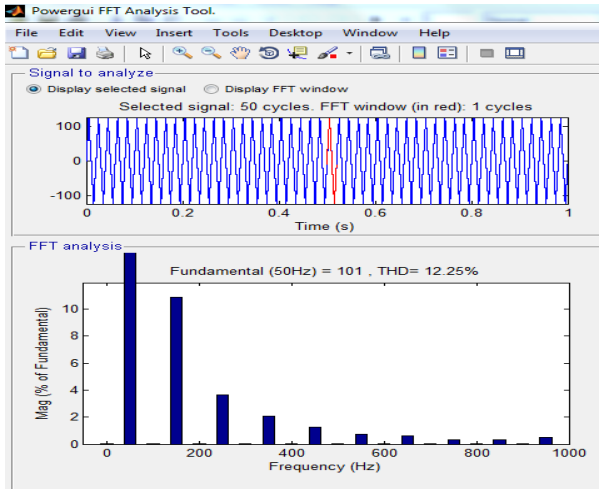


Fig.5.Experimental result 27 level

33 LEVEL SIMULATIONS AND OUTPUT:

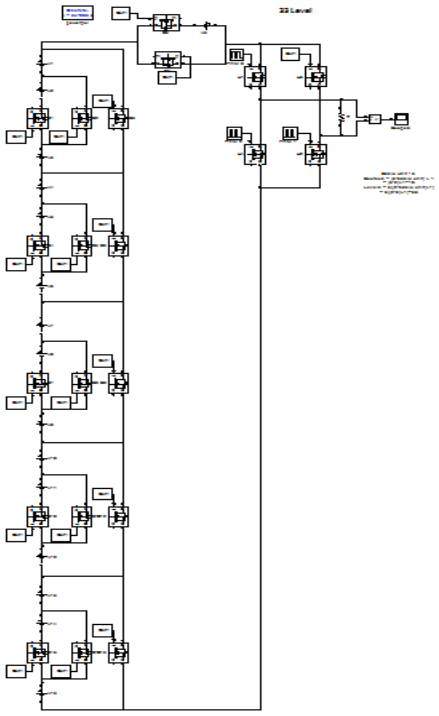


Fig.6. Proposed asymmetrical cascade multilevel inverter 33 level

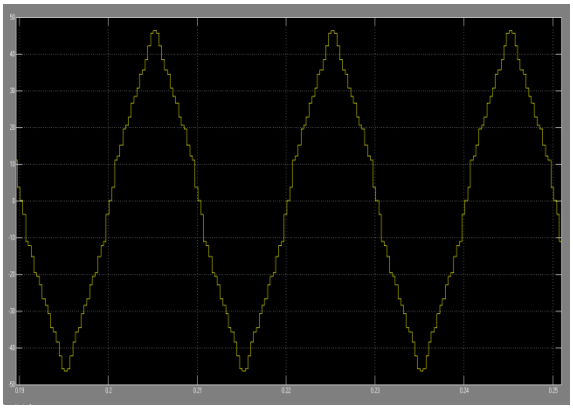


Fig.7. Simulation result 33 level

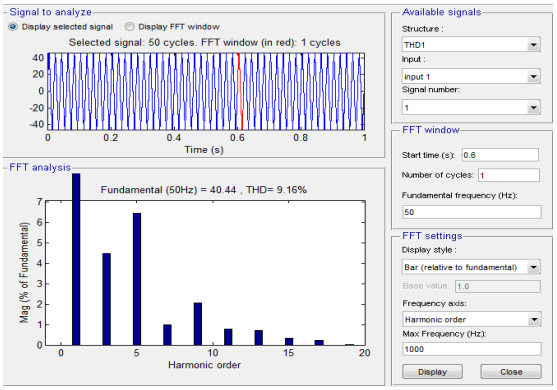


Fig.8. Experimental result 33 level

Conclusion:

The simulation results show that in this paper 3- phase 27-level and 33-level asymmetrical cascaded H-bridge inverter are studied. The output voltage of three phase Asymmetrical 27-level CHB gives 12.56% THD, whereas 33-level asymmetrical CHB gives 9.16% THD without PWM technique. Hence compared to 27-level CHB, a 33-level unequal de voltage ratio consists of minute number of harmonics and increased output voltage quality. Finally the proposed system is future industrial and automotive applications and the simulation results are shown in.

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