A Novel Approach for Fully Integrated Three-Level Isolated Single -Stage ac/dc PFC Converter for Low Power Applications

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Abstract— For low-cost isolated ac/dc power converters adopting high-voltage dc-link, research efforts focus on single-stage multilevel topologies. This project proposes a new single-stage three-level isolated ac/dc PFC converter for high dc-link voltage low-power applications, achieved through an effective integration of ac/dc and dc/dc stages, where all of the switches are shared between two operations. With the proposed converter and switching scheme, input current shaping and output voltage regulation can be achieved simultaneously without introducing additional switches or switching actions. In addition, the middle two switches are turned on under zero current in discontinuous conduction mode operation, and the upper and bottom switches are turned on under zero voltage. Due to the flexible dc-link voltage structure, high power factor can be achieved at high line voltage. A 500 W/48V is designed to serve as the proof of concept, which exhibits 90.8% peak efficiency at low input line voltage.

Index Terms— single-stage converter, three-level converter, variable dc-link voltage, zero-current switching, zero-voltage switching.

I. INTRODUCTION

A first stage ac/dc PFC converter is worked with a switching frequency in the range of tenths to a few hundred kHz for converters made up of Si semiconductors, and from a few many kHz to tenths of MHz with wide-band crevice devices, to make the shape of the input current near sinusoidal waveform in phase with the grid voltage. The second stage dc/dc converter gives the galvanic separation and yield voltage control. The controllers of the two stages are totally independent. The adaptability in control permits enhancing power stages, quick yield voltage regulation and working with high PF and low THD. But due to extra components and big size this method is expensive. In addition the efficiency of the converter has become low at light load condition because of constant switching losses like parasitic capacitance losses. To reduce the cost of the system the number of switches involved in ac/dc converter. The capacitor or inductor unit placed between two stages will act as a power buffer. Numbers of PFC ac/dc single stage technologies have been discussed in literature, especially in PFC converter with discontinuous conduction mode. These are mainly focussed towards the low power appliances, where to produce sinusoidal input current waveform and for voltage regulation a flyback converter is used. Even though they give solution for low cost device, the voltage current stresses on the switching device are more. So these converters are applicable for low power ranges less than 200 W. Appliances which operates at medium or high power, more research works focused towards ac/dc single stage full bridge (SSFB) converters. There are two types of SSFB converters, one is Current fed SSFB and the other one is Voltage fed SSFB. In current fed SSFB to shape up the current one inductor has been employed in the input side of diode bridge and power factor is high. Since there is no dc bus capacitor on the primary side of the transformer, overshoots occur in the dc bus voltage. This drawback is not occurred in Voltage fed SSFB, because of the capacitor connected on the primary side. The proposed methodology gives solution and give maximum efficiency for low input voltage.

For medium to high power applications, the research efforts have focused on ac/dc single-stage full-bridge (SSFB) converters. Current-fed SSFB converters deploy a current shaping inductor connected to the input of the diode-bridge achieving high PF; however, due to the lack of dc bus capacitor on the primary side of the transformer, the dc bus voltage is subjected to excessive overshoots and ringing. Furthermore, the output voltage contains high amplitude second-order harmonic oscillating with twice the line frequency, which restricts their operation. Voltage-fed SSFB converters do not exhibit the drawbacks of current-fed SSFB converters, where a large capacitor is located on the primary side dc bus. However, the dc bus voltage remains unregulated and it can be excessive at light load condition, as both input current shaping and output regulation are achieved with a single controller. In the literature, resonant converters adopting variable switching frequency have been proposed. In these converters, it is difficult to tune the resonant tank components over a wide load range, and optimize EMI filter. In majority of these aforementioned converters, the output current ripple becomes very large and the converter operation may transit to DCM mode.
In two-level SSFB converters, the switches are exposed to high voltage stresses; thus, dc-link voltage is typically set close to 400V. In multilevel configurations, the voltage stresses across the switches are significantly reduced. Quite recently, single stage three-level (SSTL) converters have been studied, which allow a flexible dc-link voltage in the range of 400 to 800 V. In and a resonant SSTL converter is proposed to alleviate the drawbacks associated with SSFB converters, while reducing the voltage stress on the switches. In a recent publication, a three-level converter is integrated with the PFC boost stage by sharing the bottom switch. It is aimed to decouple the dc bus voltage and output voltage controllers, while the input current is adjusted with a constant duty cycle in DCM mode. The duty cycle of the bottom switch shapes the input current as well as is used to transfer energy from dc bus to output, simultaneously. The required duty cycle is the sum of the values achieved from individual PI controllers. The output voltage regulator sets the base duty cycle, while the PI controller of dc bus voltage regulator extends the duty cycle for the bottom switch. This topology alleviates most of the problems associated with SSFB converters, operated at constant switching frequency with a flexible dc-link voltage. However, two auxiliary diodes are added to 1) prevent input current to flow through the midpoint of split dc bus capacitors, and 2) enable a freewheeling path for primary side current when the energy in the leakage inductance is transferred to the bottom capacitor. In addition, a third auxiliary diode is added to serve as a boost PFC diode.

Although the converter proposed in has been proven to work, it can further be integrated for lower power applications by removing the auxiliary diodes and developing a phase shifted modulation scheme.

The proposed converter offers minimum number of components as of three-level dc/dc converter, and does not require any auxiliary circuit other than a diode bridge and an inductor. The proposed topology can serve as a low cost power electronic interface intended for applications requiring high-voltage dc link.

Two independent control algorithms, embedded in a single microcontroller, are used to achieve PFC and output voltage regulation. This feature allows having lower output current ripple and less distorted input current even at light load condition. In addition, the middle two switches are turned ON under zero current in DCM operation, and the upper and bottom switches are turned on under zero voltage, which increases the efficiency of the converter in comparison to hard-switched ac/dc single-stage converter. Furthermore, higher PF can be achieved at high line voltage due to the flexible dc-link voltage structure.

II. PROPOSED THREE-LEVEL SINGLE-STAGE PFC CONVERTER

The proposed converter is essentially an integrated version of a boost PFC circuit and three-level isolated dc–dc converter. Basically, a diode bridge and an inductor are added to the three-level isolated dc–dc converter topology as shown in Fig.2.1(a). Here, the inductor is charged when S2 and S3 are turned on simultaneously. Body diodes of S1 and S4 serve as the boost diode of the PFC boost converter. At the same time, S1 to S4 are switched to apply Vdc/2, −Vdc/2, and zero voltage across the primary side of the transformer. Thus, all of the switches are shared between the two-stages, which makes it fully integrated single-stage converter without any additional auxiliary switches. The switching scheme of the conventional three-level isolated dc/dc converter is given in Fig. 2(b). In this conventional scheme, the duty ratios of S2 and S3 are fixed close to 50% for simplicity in control and to ensure upper or lower three switches are not turned ON simultaneously as this would cause short-circuit through dc-link capacitors. Overlapping these two signals, as long as short-circuit condition is avoided, has no impact on the operation of the circuit. Similar to that in the conventional scheme, zero voltage is applied across the primary side of the transformer. This modified switching scheme is presented in Fig.2.1(c). When a boost inductor and a diode bridge is added to the nodes as in Fig.2.1(a), the overlap of gate signals of S2 and S3 enables applying input voltage across the boost inductor.

The switching scheme of the converter is given in Fig. 2. The switches S2–S3, and S1–S4 have 180° phase shift with respect to each other. The duty ratios of S2–S3 should be greater than 0.5 such that two signals
overlap. Here, the circuit is explained considering that input inductor current is discontinuous and the switching scheme is as follows; S1 is turned on right after S3 is turned OFF, and similarly, S4 is turned on when S2 is turned OFF. A dead-time should be inserted in between the turning ON instant of S1 and turning OFF instant of S3, and likewise between switching of S2 and S4 to avoid short-circuit.

**III. CONVERTER FEATURES**

The proposed converter has the following advantages over the state-of-the-art two-stage PFC converters.

1) **Less Number of Switches/Diodes:** The proposed converter has the same number of switches as of three-level isolated dc/dc converter, and achieves high PF operation with only changing the switching scheme. Only a diode-bridge and a boost inductor are added to the dc/dc stage. No additional switches/diodes or switching actions have been introduced in comparison to other SSTL topologies. However, due to inherent three level structure, it constitutes more components in comparison to SSFB topologies.

2) **Flexible DC-Link Voltage:** Since the proposed single-stage converter is essentially derived from a three-level converter, the voltages across the switches are halved in comparison to that of the full-bridge derived or two-stage topologies. This brings more flexibility in choosing the dc-link voltage and thereby, designing the parameters. At high dc-link voltage, the efficiency of the converter decreases in DCM; however, as it is analyzed in the following section, higher dc-link results in achieving higher PF. The loss mechanism is introduced and this tradeoff is addressed.

3) **High Power Factor:** In accordance with the previous feature, higher PF can be maintained with higher dc-link voltage in the case that the input current is discontinuous. When the converter is operated at a constant duty ratio, the peak current follows a sinusoidal envelope as \( v_{in}(t) \) is applied across the input inductor terminals and the input voltage is sinusoidal, as shown in Fig. 5. Hence, the averaged current value within a switching period also has sinusoidal waveform. However, when the switch is turned OFF, constant dc bus voltage is applied to the inductor terminals. Therefore, the turning off current averaged over the switching period does not follow the sinusoidal envelope. When the dc-link voltage is higher, the slope of the decreasing current is also higher so that the current averaged over the switching period is closer to sinusoidal envelope. The following mathematical relations illustrate the derivation.

The input voltage can be expressed as

\[
 v_{in}(t) = V_m \sin(\omega t) \tag{1}
\]

where \( V_m \) denotes the peak value of the sinusoidal input voltage.

4) **Independent Controllers:** Although the proposed converter is single-stage, the control of the converter is similar to two-stage converters, where the input current shaping and output voltage regulation operations are performed by independent controllers. This flexibility makes the design of the converter simpler in comparison to single controller-based single-stage converters, since the dc-link voltage can be regulated at a determined value.

5) **Light Load Efficiency:** At light load, the constant losses such as parasitic capacitance losses are dominant as they are independent of load power. In comparison with the two-stage PFC converters, the constant losses are lower as there is less number of switches and the voltage across the switches are halved.

6) **Doubled Input Current Ripple Frequency:** Since the overlap of gate signals of S2 and S3 occur twice within a switching period, the input inductor current ripple frequency is twice of the switching frequency, which
in-turn allows using a smaller inductor. In addition, since the frequency of the input current ripple is shifted by two times, required EMI filters are smaller.

7) Low Power Operation: The proposed converter has a limitation on the duty cycle as will be presented in (18), in latter sections. This limitation can be interpreted as the sum of the on time of the switches should be less than the switching period, \( T_s \), which dictates a constraint on the converter design. For a given output power requirement, \( D_1 \) can be constrained to any value less than 0.5. Taking into account (12), there are always finite values of \( L_b \) and \( f_s \) that can meet the requested power to be injected to the dc-link. With properly chosen parameters, the converter can be designed and operated at any power level. Similarly, the maximum value of \( D_2 \) can be found by \( 0.5 - D_1 \). The turns ratio that can provide the determined \( D_2 \) can be found using (16) and (17) that are given in latter sections. However, transferring high power in DCM mode will result in higher core and conduction losses due to the significantly high peak current and flux density, which in turn diminishes the efficiency. Because of this reason, the converter is suitable for low power levels where high dc-link voltage and lower cost are essential requirements.

IV. CONVERTER ANALYSIS

The analysis and design of the proposed converter are almost identical to that presented in [16] and [17] and therefore are not presented here in detail. Only graphs of key characteristic curves and general design guidelines are presented in this paper. The reader is referred to [16] and [17] for details. In order to analyze and determine the steady-state operating points of the converter, a computer program such as the one presented in [16] has been used. Graphs of steady-state characteristics, such as the ones shown in Fig. 6, can be used as part of a design procedure.

These graphs help to find out the appropriate parameter values based on the defined operating point. Assuming ideal operation to simplify the analysis, the characteristic curves of the proposed converter and the converter proposed in [17] are the same. This is because in this case, the flying capacitor just affects the transition modes of the converter and does not affect the overall steady-state operation of the proposed converter.
Fig. 6 Steady-state characteristic curves (Vin = 208 Vrms, Vo = 48 V, fsw = 100 kHz) (a) Effect of output inductor value Lo on dc bus voltage (b) Effect of input inductor value Lin on dc bus voltage (c) Effect of transformer ratio value N on dc bus voltage (d) Effect of input voltage vin on dc bus voltage

V. SIMULATION RESULTS
A simulation design of the proposed three-level converter and the converter shown in Fig. 1 were built to compare their performance.

Fig. 5.1 MATLAB simulation diagramm of proposed three-level single-stage fully integrated PFC ac–dc converter

Fig. 5.2 simulated waveforms: Input voltage, input current, dc-link voltage

Fig. 5.3 simulated waveforms: Input voltage, input current

Fig. 5.4 simulated waveforms: Transformer primary side voltage and current
Fig 5.5 simulated waveforms: Output inductor voltage output inductor current

CONCLUSION

In this project, a three-level single-stage PFC ac/dc converter is proposed for low-power applications. The proposed converter exhibits high PF with less number of switches/diodes, operated at constant duty ratio. A PFC inductor and a diode bridge are added to the conventional three-level isolated dc/dc converter, while the switching scheme is modified to be compatible with single-stage operation. The input current ripple frequency is twice of the switching frequency contributing to using smaller PFC inductor. Two independent controllers, in favor of shaping the input current and regulating the output voltage, are adopted which simplifies the design and control of the circuit. The tradeoff between the PF and overall efficiency in the case of adopting a variable dc-link voltage is analyzed through developed loss model. The results of the analyses show that under 265 V line voltage, the PF can be increased to 0.99 from 0.88 by varying the dc-link voltage from 400 to 800 V. On the other hand, the efficiency of an 800 W/48 V converter can drop from 95.2% to 90% at full load. A 500W system has been designed to serve as a proof concept achieving a peak efficiency of 90.8% at low input line voltage.

REFERENCES


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